High-reliability programmable CMOS WTA/LTA circuit of $O(N)$ complexity using a single comparator

Y.-C. Hung and B.-D. Liu

Abstract: A high reliability complementary metal–oxide–semiconductor (CMOS) winner-takes-all/loser-takes-all circuit of $O(N)$ complexity with programmable capability is designed. Based on the proposed architecture, the precision of the circuit is independent of the number of inputs. This circuit is easily programmed for WTA or LTA function by an enable signal, without modifying the circuit structure or preprocessing the input variables. Since the circuit contains only simple logic gates and a single comparator, it is tolerant of VLSI process variations. The response time of the circuit increases linearly with the number of inputs. The input signal range of the circuit allows rail-to-rail (0–V_{DD}) operation. The supply voltage ranges from 2.7 V to 5 V. An experimental chip with six inputs was fabricated using 0.5-μm CMOS double-poly double-metal technology. The results show that a cell is either a winner or a loser if its input voltage is larger or smaller than the other cells by 10 mV.

1 Introduction

Winner-takes-all (WTA) and loser-takes-all (LTA) circuits are the major function blocks in pattern classification, optimisation problems, and self-organising neural networks [1, 2]. The function of a WTA (or LTA) circuit identifies the largest (or the smallest) input variable and inhibits the remaining ones. Many analogue circuits have been proposed, in which some circuits have current signals as input [3–8], whereas the others' inputs are voltage signals [9–15].

In general, these traditional circuits can roughly be grouped as: (i) global-inhibition structure [2, 3], [9, 12–14], in which the connectivity increases linearly with the number of inputs; (ii) cell-based tree topology [5, 7]; (iii) excitatory/inhibitory connection [11]; (iv) serial cascade structure [15]. Figure 1 shows the conceptual diagrams of these topologies. In Fig. 1*a*, each cell receives the same global inhibition, and a common current I_{comn} or voltage V_{comn} is shared by all the cells. The cell represented in a square block is a nonlinear signal-processing element. In this architecture, the precision of the circuit is degraded as the number of inputs increases. Since the operation of this circuit relies on the cells matching, a stable fabrication process is required for manufacturing a high-precision system. The complexity of the connectivity of the circuit is $O(N)$, where N is the number of inputs. Figure 1*b* shows a cell-based tree topology, with $N-1$ cells arranged in a tree topology for N inputs. Each cell receives two input variables to compare and outputs the larger (or smaller) of the two input signals. The backward digits in the bottom cell are then successively fed back to the first layer to identify the maximum (or minimum) input. The precision of the circuit is sensitive to cells matching. Figure 1*c* shows an excitatory/inhibitory connection with $O(N^2)$ complexity. Each cell receives the inhibited signals from other cells and an excitatory signal from itself. With this design, chip area increases with the square of the number of inputs. Based on 'many comparators' operation, Fig. 1*d* shows $N-1$ analogue comparison blocks and $N-1$ digital blocks cascaded in series. Within a comparison time T_{comp}, the largest magnitude input in each analogue block is sent to the next stage to compare with other inputs. The result of each comparison is then sent to the corresponding digital block, and a decision digit is fed back from right block to left block to identify the maximum input. As a result, the response time of the circuit is approximately $(N-1)\cdot T_{comp}+T_{dig}$, where T_{dig} is the total propagation time of the digital part. The precision of the architecture is dominated by the worst offset of the comparators. The major limitations of these conventional architectures are the fabrication process variations and the matching requirements of internal cells. The variations of a CMOS fabrication process include the transistor threshold voltage, actual device size, thickness of the gate oxide, and a variety of other factors. Analogue circuits are sensitive to these effects, especially for high-precision designs.

In this paper, a new high-reliability WTA/LTA architecture with wide input range and an adjustable supply voltage is proposed. The conceptual diagram of the circuit is shown in Fig. 2. In the proposed scheme, there are N identical control cells and a single comparator for N input variables. A comparator block multiplexes in time to achieve comparison of all inputs, and the comparator block itself is realised using an auto-zero technique. The WTA/LTA circuit is composed solely of basic elements; these include latches, inverters and logic gates. Since there are no critical elements in this design, performance of the circuit is stable with respect to variations in CMOS manufacturing.

2 Operating principle and circuit design

2.1 Operating principle

A symbol $COMP_i^j(V_{inj}, V_{ink})$ $(1\leqslant j, k\leqslant N)$ is defined such that the ith comparator cell receives two input variables (V_{inj}

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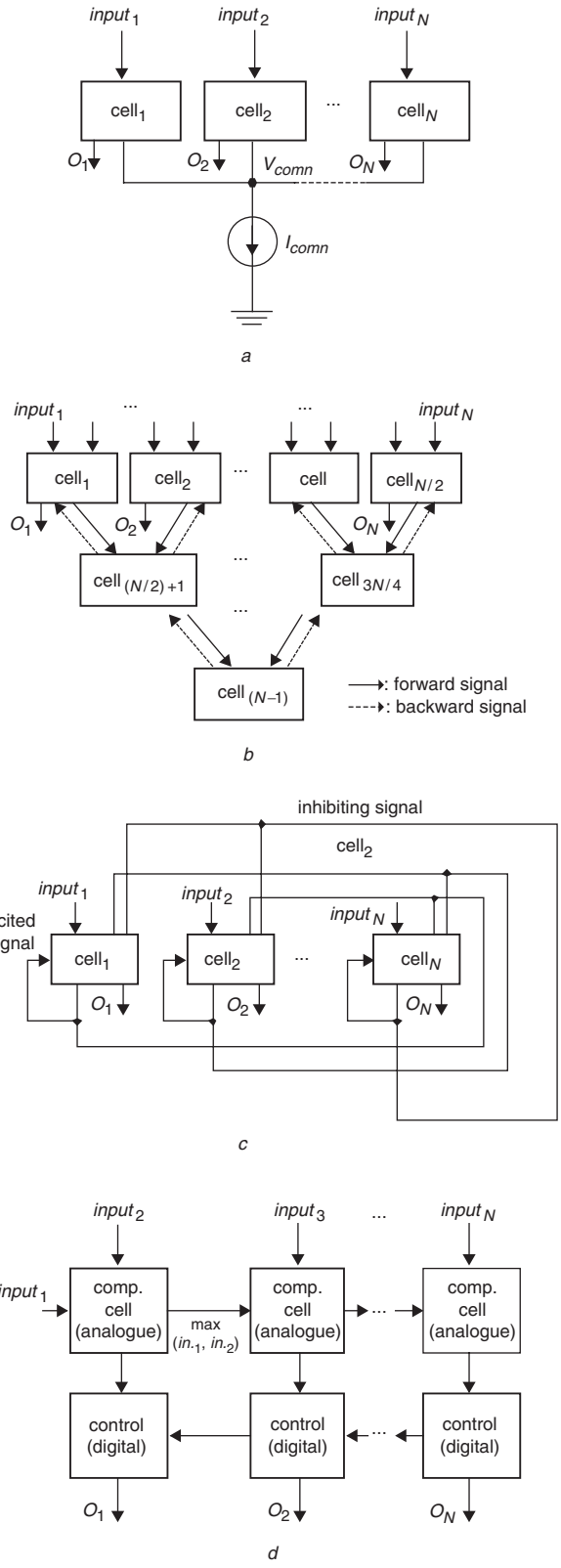

Fig. 1 *Different topologies*
a Global-inhibition structure
b Cell-based tree-topology
c Excitatory/inhibitory connection
d Serial cascade

and V_{ink}) to compare in magnitude at time t, and the output Z_t^i of the cell is the larger variable or a binary value. For $COMP_t^i(V_{inj}, V_{ink})$ operation, Z_t^i is defined as

$$z_t^i = \begin{cases} 1 \text{ or } V_{inj}, \text{ when } V_{inj} > V_{ink} \\ 0 \text{ or } V_{ink}, \text{ otherwise} \end{cases}$$

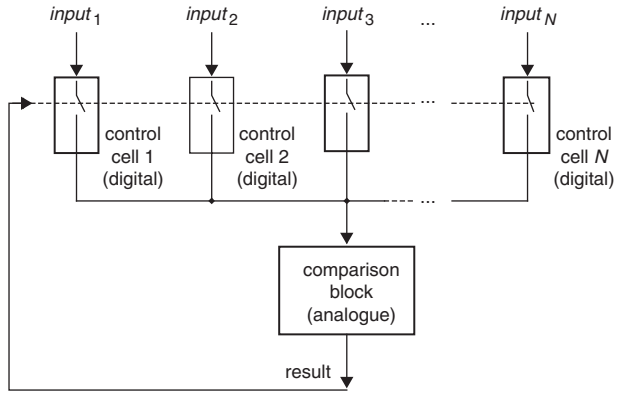

Fig. 2 *Proposed architecture using a single comparator*

Therefore, the tree topology of Fig. 1*b*, WTA mode, is represented as

$$t_1 : COMP_{t1}^1(V_{in1}, V_{in2}),\ COMP_{t1}^2(V_{in3}, V_{in4}),\ COMP_{t1}^{N/2}(V_{in(N-1)}, V_{inN})$$
$$t_2 : COMP_{t2}^{(N/2)+1}(Z_{t1}^1, Z_{t1}^2),\ COMP_{t2}^{(N/2)+2}(Z_{t1}^3, Z_{t1}^4), \ldots$$
$$\vdots$$
$$t_{(\log_2 N)} : COMP_{t_{(\log N)}}^{(N-1)}(Z_{t_{(\log N)-1}}^{N-3}, Z_{t_{(\log N)-1}}^{N-2})$$

After time $O(\log_2 N)$, the maximum input variable is obtained. $N-1$ identical comparators are necessary for this operation. Figure 2 shows the proposed topology and uses a single comparator to accomplish the whole operation. The operating procedures are described as follows:

$$t_1 : COMP_{t1}^1(V_{in1}, V_{in2})$$
$$t_2 : COMP_{t2}^1(Z_{t1}^1, V_{in3})$$
$$\vdots$$
$$t_{(N-1)} : COMP_{t(N-1)}^1(Z_{t(N-2)}^1, V_{inN})$$

Since the required minimum time in each comparison step is different, each time interval must be designed as the worst value among all comparisons. The strategy adopted to find the maximum/minimum among a set of variables is that two variables are first compared; then the result of this comparison is compared with the next input variable using the same comparator. The procedure continues until comparisons of all input variables are completed. The single comparator operates in sequential time steps to compare different input levels. The comparison mode of the architecture is thus changed to a discrete time operation. Conceptually, circuit operation is similar to serial comparison. Unlike the traditional architectures that require $N-1$ comparators, this architecture requires only a single comparator. Using the algorithm described earlier, the LTA function is easily obtained by reversing the output state Z_t^i in the same architecture.

2.2 Comparator

A comparator design from [16] is used herein; the schematic diagram is shown in Fig. 3. Transistors M_{sw1}, M_{sw2}, M_{sw3} are used as switches. The circuit operates in two phases, the auto-zero phase and the comparison phase. Initially, in the auto-zero phase, clock V_{s1} becomes high to sample V_{in1}. Meanwhile, switch M_{sw3} is closed; therefore the first inverter is biased at V_b . At this time, the amount of electric charge Q_{B1} at node B is expressed as

$$Q_{B1} = (V_b - V_{in1}) \cdot C_s + V_b \cdot C_p + V_b \cdot C_{in} \qquad (1)$$

where C_s , C_p and C_{in} are the sampling capacitance,

parasitic capacitance of the bottom plate of C_s, and input capacitance of inv-1, respectively.

In the comparison phase, assuming the voltage at node B at this time is V_x,. V_x is the meta-stable voltage for the comparator. The amount of electric charge Q_{B2} at node B is expressed as

$$Q_{B2} = (V_x - V_{in2}) \cdot C_s + V_x \cdot C_p + V_x \cdot C_{in} \qquad (2)$$

Based on charge conservation, Q_{B1} in (1) and Q_{B2} in (2) must be equal, so that

$$V_x = V_b + (V_{in2} - V_{in1}) \cdot \frac{C_s}{C_s + C_p + C_{in}}$$
$$= V_b + \Delta V_{in} \cdot \alpha \qquad (3)$$

where ΔV_{in} represents the level difference of the two inputs, and $\alpha = C_s/(C_s + C_p + C_{in})$, which represents a degrading factor. The function of the N-latch is to sample the voltage at node D as *latch_clk* sets high, and to hold the comparison result as *latch_clk* sets low. The *max/min selector* signal modifies the polarity of the compared result; therefore, without the need for structural modification, this circuit possesses a win/lose configurable capability. The dashed block in Fig. 3 shows the comparison block, which is used for all comparison procedures.

2.3 Architecture

The architecture of the N-input circuit is shown in Fig. 4, in which the N cells control_cell$_n$ ($1 \leqslant n \leqslant N$) are identical. These cells are arranged in serial form, and N cells are required for N input variables. Each cell contains a status block, control_switch block, and latch blocks. The status block is designed to indicate whether the corresponding input variable is the winner or the loser. A following-inhibit signal (*fol_inhibit*) from the following cell is used to reset the status block, and an output inhibit signal (*inhibit*) is propagated to the preceding cell. The control_switch block receives an input variable and feeds this variable to the comparison block at the proper moment. Two input signals from following cell (the following-inhibit-switch signal

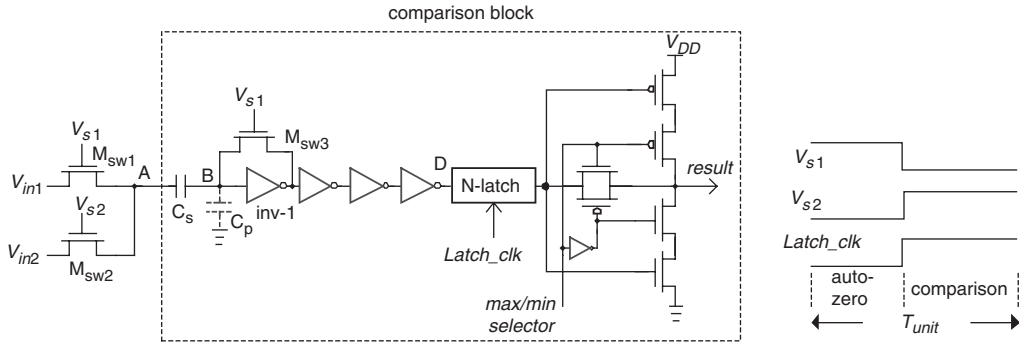

Fig. 3 *Comparison block and control signals*

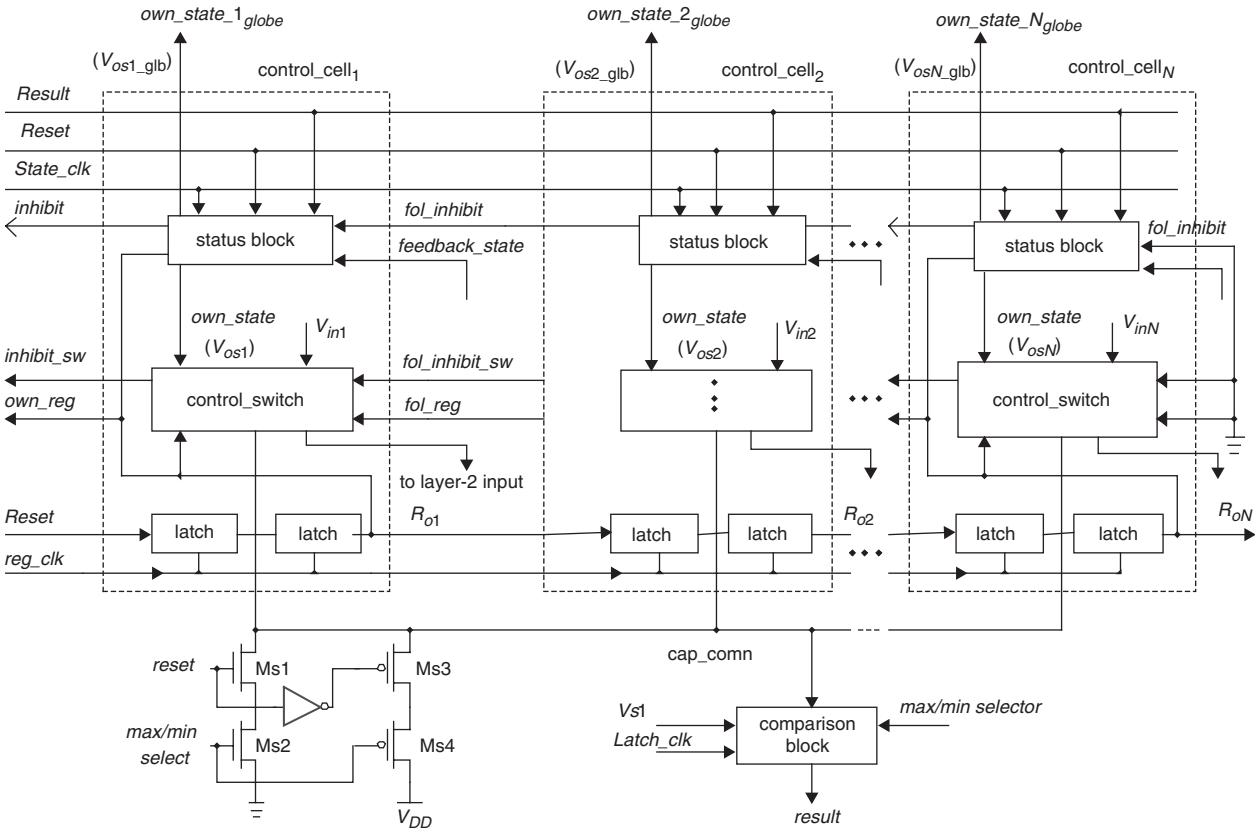

Fig. 4 *Architecture of the whole circuit*

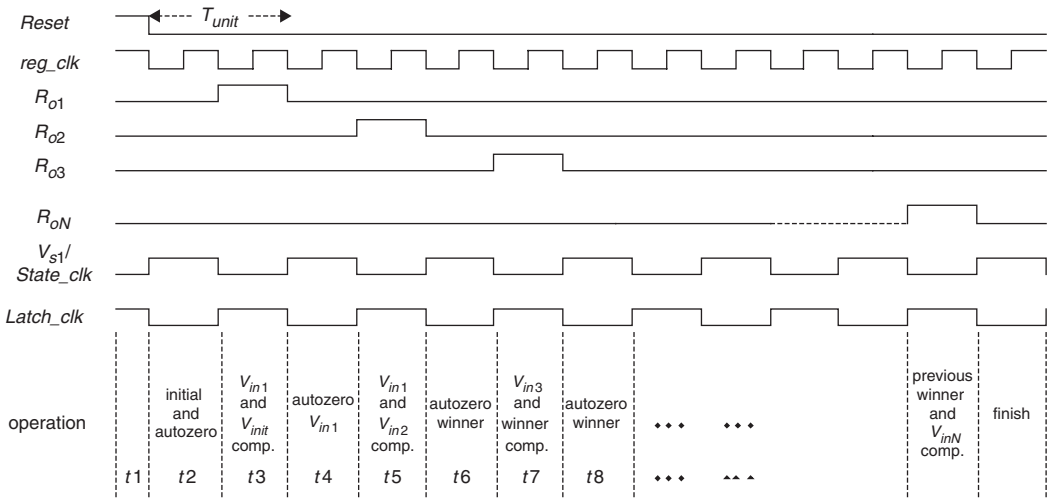

Fig. 5 *Clock waveforms*

(*fol_inhibit_sw*) and the following-register signal (*fol_reg*)) are used to generate a sampling period. Two output inhibiting signals (*inhibit_sw* and *own_reg*) are used to inhibit or retain the winner's status in the preceding cell. Figure 5 shows clocks for the whole circuit.

2.4 Whole operation

The operation of the entire circuit is described using the circuit architecture in Fig. 4 and the clock waveform in Fig. 5. First, at $t1$, the *reset* signal is used to initiate the status blocks, control_switch blocks, and latch blocks. The N-latch in the status block and R_{o1}, R_{o2}, …, R_{oN} are reset to zero by the *reset* signal. Based on the *max/min selector* signal, MOS transistors Ms1, Ms2, Ms3, and Ms4 preset the initial sampling voltage (0 V or V_{DD}) at node cap_comn. Regardless of the magnitude of the input-1 variable, it must be a winner during the initial interval for a serial comparison. The initial sampling voltage at node cap_comn is thus set as 0 V when the *max/min selector* signal is set to logic 1 for WTA operation, and *vice versa*.

Then, at $t2$, V_{s1} clock becomes high (auto-zero phase) to sample the initial voltage (0 V or V_{DD}) at node cap_comn. Next, at $t3$, R_{o1} becomes high to sample voltage V_{in1}. At this time, clock V_{s1} becomes low (comparison phase) to compare V_{in1} with the initial sampling voltage, and the result of the comparison is stored in the N-latch of the first status block. The state of the N-latch is logic 1 if the variable is the winner. At $t4$, the present winner V_{in1} is sampled again. At $t5$, a new comparison between previous winner V_{in1} and V_{in2} is made. At $t6$, the winner (the result of the V_{in1} and V_{in2} comparison) is sampled again. Then, a new comparison between the present winner and V_{in3} is performed. The procedure continues until comparison of all the input voltages is completed. Ultimately, only one state V_{osn} ($n = 1, \ldots, N$) in these cells is at logic 1 for WTA/LTA indication; all others are at logic 0. Therefore, a WTA or LTA operation has been accomplished.

2.5 Block circuit description

Status block: Figure 6 shows the status block. The N-latch is used to store the result of the comparison (binary voltage V_{osn}). V_{osn} logic high means that the corresponding input variable is currently either a winner or a loser for WTA/LTA operation. The shaded part of the circuit is designed for a two-layer architecture, and will be discussed in Section 4.

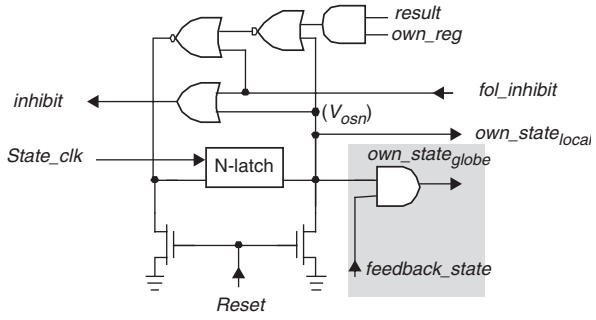

Fig. 6 *Status block*

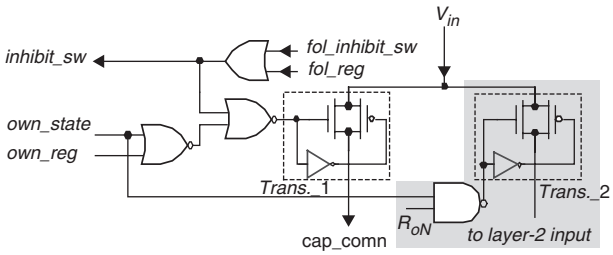

Fig. 7 *Control_switch block*

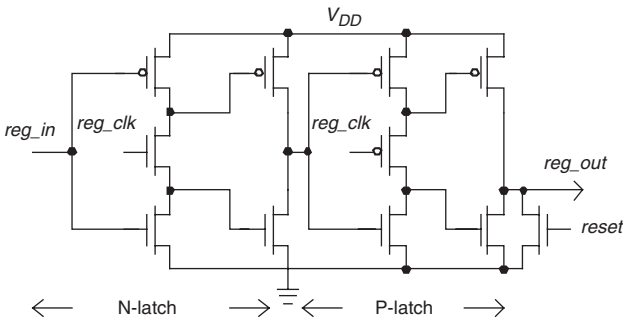

Fig. 8 *True single-phase latch stage*

Control_switch block: Figure 7 shows the control_switch block. It receives an input variable and controls the transmission gate to sample input variable. The shaded part in the figure is used in a two-layer architecture.

Latch Block: Figure 8 shows the latch block [17]. The latch circuit is composed of an N-latch and a P-latch. By using a single-phase clock *reg_clk*, there is no clock skew in the circuit.

2.6 Design consideration

The accuracy of the comparator cell dominates circuit precision. The accuracy of the comparator is dependent on two factors: one is the clock feedthrough error and charge-injection error in transistor M_{sw3}, shown in Fig. 3 and the other is the degrading factor in (3). The charge-injection error is a complicated function of substrate doping concentration, load capacitor, input voltage, clock voltage, clock falling rate, MOS channel dimension, and threshold voltage. Therefore, this error is difficult to completely eliminate. Charge Q_{overlap}, induced by the lateral diffusion of channel length, and charge $Q_{\text{inversion}}$, induced by the channel inversion layer, are the primary error sources. First-order analysis of the error voltage gives

$$E_{err} \propto \frac{Q_{overlap} + Q_{inversion}}{C_s + C_{in} + C_p} = \frac{V_{DD} \cdot C_{ox} \cdot W \cdot L_D + \chi \cdot (V_{DD} - V_{th}) \cdot C_{ox} \cdot W \cdot L}{C_s + C_{in} + C_p}, \quad (4)$$

where C_{ox}, W, L_D, and χ are the gate oxide capacitance per unit area, channel width, lateral diffusion length, and fractional part of the charge leaving the MOS transistor M_{sw3}, respectively [18, 19]. In general, a complementary clock, transmission gates, and dummy transistors are adopted for switch realisation to reduce the error. Based on (3), the parasitic and input capacitances degrade the effective magnitude of the differential voltage ($V_{in2} - V_{in1}$). Therefore, circuit resolution decreases as parasitic capacitance C_p and input capacitance C_{in} increase. Accordingly, precision can be improved by increasing the sampling capacitance C_s and reducing the dimensions of the first inverter (Fig. 3). In contrast with accuracy considerations, the settling time of the input signal during the sampling phase can be reduced by using a transmission gate (M_{sw3} in Fig. 3) having smaller on-resistance or smaller sampling capacitance (C_s in Fig. 3) to improve the speed. The trade-off is between circuit accuracy and circuit operating speed.

3 Simulation and measurement results

WTA/LTA functions, supply-voltage range, and Monte Carlo analysis of transistor variation were tested by simulation to verify the performance of the circuit. An experimental chip with six inputs was fabricated using 0.5 μm CMOS double-poly double-metal technology.

3.1 WTA/LTA functions

To test the functioning of the circuit, each example takes ten input voltages for WTA/LTA operation. For supply voltage $V_{DD} = 3.3$ V, the input variables (V_{in1}, V_{in2}, …, V_{in10}) are (0.003, 0.006, 1.000, 0.997, 2.000, 2.003, 2.000, 3.297, 3.300, 3.297 V) to test WTA function, and (3.297, 3.294, 2.000, 1.997, 2.000, 1.000, 0.997, 0.006, 0.009, 0.003 V) to test LTA function. During WTA operation, the logic V_{osn} of each cell at each time slice becomes:

$V_{os1} = 1,0,0,0,0,0,0,0,0,0$ $V_{os2} = 0,1,0,0,0,0,0,0,0,0$
$V_{os3} = 0,0,1,1,0,0,0,0,0,0$ $V_{os4} = 0,0,0,0,0,0,0,0,0,0$
$V_{os5} = 0,0,0,0,1,0,0,0,0,0$ $V_{os6} = 0,0,0,0,0,0,1,1,0,0,0$
$V_{os7} = 0,0,0,0,0,0,0,0,0,0$ $V_{os8} = 0,0,0,0,0,0,0,0,1,0,0$
$V_{os9} = 0,0,0,0,0,0,0,0,1,1$ $V_{os10} = 0,0,0,0,0,0,0,0,0,0$

When all comparisons are completed, logic (V_{os1}, V_{os2}, V_{os3}, ..., V_{os10}) = (0, 0, 0, 0, 0, 0, 0, 0, 1, 0). Therefore, among these ten inputs, input voltage V_{in9} is the maximum. Figure 9 shows the results of HSPICE simulation for WTA operation. The period of the latch clock (top trace) is 100 ns. For LTA operation, the final logic (V_{os1}, V_{os2}, V_{os3}, …, V_{os10}) is (0, 0, 0, 0, 0, 0, 0, 0, 0, 1), and the input voltage V_{in10} is the minimum variable. Choice of the above test voltages was based on the following: (i) input voltages of neighbour cells should be as close as possible to test discrimination capabilities; (ii) input voltages are distributed from 0 V to 3.3 V to test over a wide input range.

3.2 Supply voltage range

All circuit parameters, such as transistor dimensions, clock periods and sampling capacitance C_s are held constant. Supply voltage V_{DD} varies from 2 V to 5 V. Simulation results show that the circuit operates successfully with 3-mV discrimination over a supply voltage range from 2.7 V to

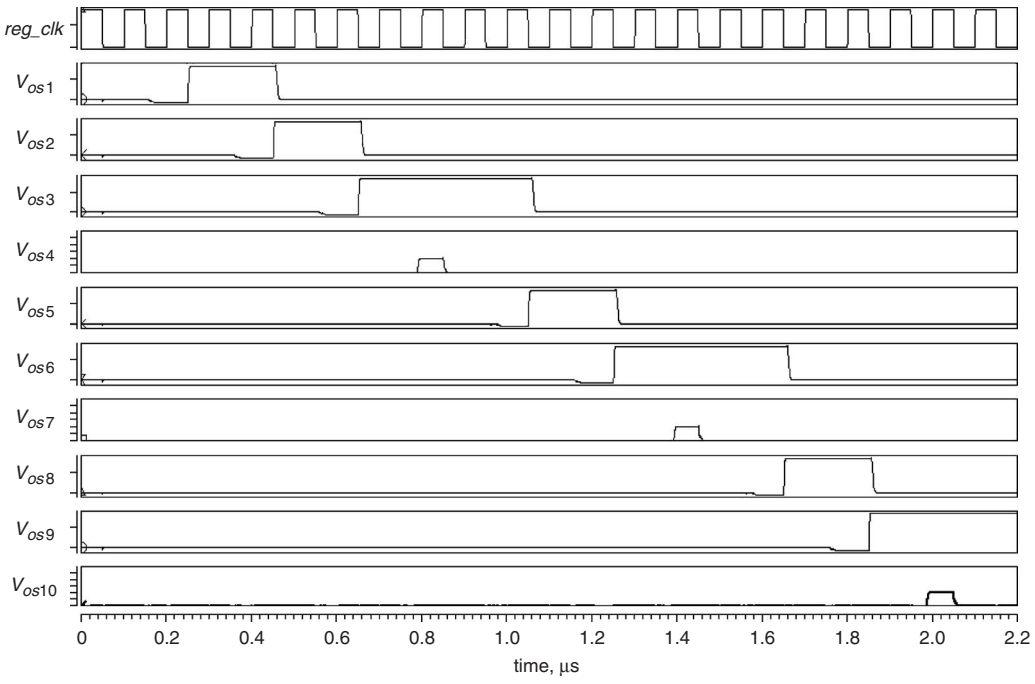

Fig. 9 *Simulation results of the circuit for WTA operation*

5 V. The unit operates under various commonly used supply voltages without any rescaling of device size.

3.3 Monte Carlo analyses of transistors – dimension and threshold-voltage variations

A statistical distribution of manufacturing parameters always occurs during CMOS fabrication. Threshold voltage, channel widths, and channel lengths of all MOS transistors were set to nominal values with ± 5 % variation at the 3σ level, and each transistor was given an independent random Gaussian distribution. After thirty Monte Carlo iterations, HSPICE results indicate that circuit precision and speed are not degraded over this range. In addition, to verify the circuit with multi-technology support capability, circuit performance was simulated for different CMOS fabrication parameters. Results show that even for different fabrication processes the circuit functions correctly without tuning device dimension.

3.4 Measurement result

Figure 10 shows a micrograph of the chip. Input variables (V_{in1}, V_{in2}, …, V_{in6}) were set at (1.00, 1.01, 2.00, 2.01, 3.29, 3.30 V) to test WTA function. For simplicity, Fig. 11 shows the clock *reg_clk* and output responses V_{os4}–V_{os6}. Obviously, V_{in6} is the winner among the input voltages. Input variables (V_{in1}, V_{in2}, …, V_{in6}) of (3.00, 2.99, 1.00, 0.99, 0.01, 0.00 V) were used to test LTA function. The measurement shows that V_{in6} is the loser. Table 1 summarises the characteristics of the circuit. Table 2 lists the results of comparisons with various circuits in the open literature.

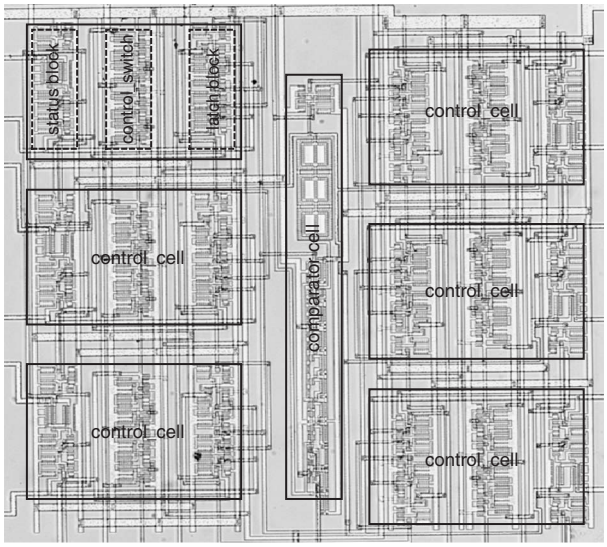

Fig. 10 *Micrograph of the chip*

4 Two-layer architecture and applications

4.1 Two-layer architecture

To further enhance performance, multiple WTA/LTA circuits can be expanded to a two-layer architecture. N inputs are divided into K groups to reduce the comparison time, each group having M input elements. Figure 12 shows a two-layer architecture consisting of a cascade of K WTA/LTA circuits at layer 1 and a single WTA/LTA circuit at layer 2. The K WTA/LTA circuits at layer 1 locate the local maximum or minimum variable among M inputs, and the result of layer 1 is sent to layer 2 to locate the global maximum or minimum. After the comparison result of layer 2 is fed back to layer 1, the maximum or minimum of voltage V_{osn_glb} ($n = 1$ to N) is found. Since these K circuits operate in parallel, the response time of the circuits at layer 1 is $M \cdot T_{unit}$ (excluding initiation time), and time $K \cdot T_{unit}$ is required for layer 2 operation where T_{unit} is a unit of time for each variable comparison. Therefore, time T for the whole circuit to accomplish WTA/LTA operation is expressed as

$$T = M \cdot T_{unit} + K \cdot T_{unit} \tag{5}$$

Furthermore, if a total number N of input variables is required, the number of circuits at layer 1 must satisfy the

Table 1: Chip characteristics

Process technology	0.5 μm CMOS double-poly double-metal
Function	WTA/LTA configurable
Supply voltage	2.7 V–5 V
Sampling capacitance	3 pF
Resolution	5 mV–10 mV
Latch clock	10 MHz
Response time	linearly increasing with number of inputs
Dynamic range	rail-to-rail
Power dissipation	850 μ at 3.3 V, 10 MHz (including I/O PAD)

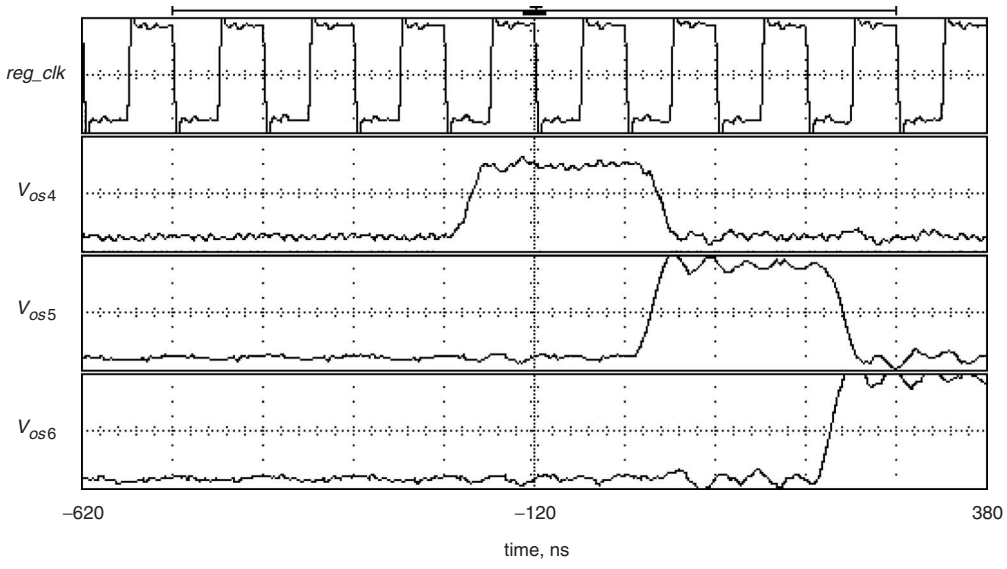

Fig. 11 *Measured results of WTA operation*

Table 2: Characteristics comparison

Circuit	Input variable	Precision	Response time	Input range	Function
[4]	current	1.5 μA (simulated)	100 ns–1.3 μs for 18 inputs (simulated)	0–100 μA	WTA
[5]	current	10 μA (simulated)	233 ns for 100 inputs (simulated)	0–100 μA	WTA
[6]	current	about 1 μA (measured)	308 ns–10.9 μs for 10 inputs (measured)	10 μA–500 μA	WTA/MAX
[7]	current	about 1 μA (measured)	233 ns for 1024 inputs	0 –100 μA	WTA
[8]	current	about 200 nA (simulated)	2 μs for 6 inputs	7 μA– 40 μA	rank order
[9]	voltage	15 mV (measured)	120 ns for 6 inputs	0 –3 V	LTA
[10]	voltage	40 mV (measured)	20 μs for 7 inputs	0–1 V	rank order and *K*-WTA
[11]	voltage	20 mV (simulated)	700 ns for 3 inputs (simulated)	N/A	LTA
[12]	voltage	15 mV (measured)	200 ns–300 ns (measured)	N/A	WTA
[13]	voltage	20 mV (measured)	50 ns (measured)	N/A	WTA
[14]	voltage	19 mV–46 mV (measured)	500 ns for 10 inputs	0–5 V	*K*-WTA
[15]	voltage	$<$10 mV (simulated)	210 ns for each input (simulated)	0.2 V – 4.4 V (5 V supply)	(i) WTA/MAX (ii) Precision is independent of *N*
This work	voltage	5 mV–10 mV (measured)	200 ns for each input (measured) 4 μs for 100 inputs (2-layer simulated)	0–V_{DD}	(i) WTA/LTA configurable (ii) precision is independent of *N* and device size (iii) multi-fabricated-process support

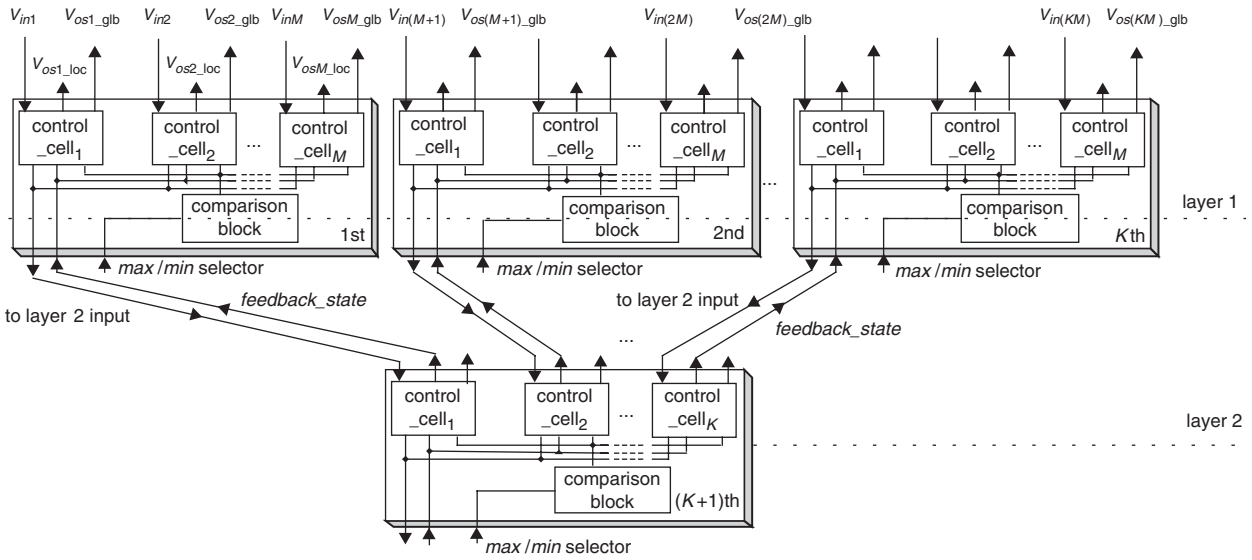

Fig. 12 *Two-layer architecture*

condition

$$K \cdot M \geq N \tag{6}$$

In order to reduce time T, the optimum number of inputs M in each WTA/LTA obtained by differentiating (5) with respect to M and using (6) to obtain

$$M = \sqrt{N} \tag{7}$$

The total response time T of the two-layer architecture is

$$T = 2 \cdot \sqrt{N} \cdot T_{unit} \tag{8}$$

Therefore the time complexity of a two-layer WTA/LTA operation is improved from $O(N)$ to $O(\sqrt{N})$.

4.2 Two-layer applications

Based on the *max/min-selector* signal setting, different two-layer configurations are set for various requirements.

(i) WTA–WTA: All the *max/min-selector* signals at layer 1 and layer 2 are set as logic 1. This indicates that the function of each layer is set as WTA, and the result is a global WTA function.

(ii) LTA–LTA: All *max/min-selector* at two layers are set at logic 0 to attain a global LTA function

(iii) WTA–LTA (LTA–WTA): The *max/min-selector* signals of layer 1 are set at logic 1, and the layer 2 signal is set at logic 0. The output of the whole system identifies the minimum among the local maxima. An LTA–WTA

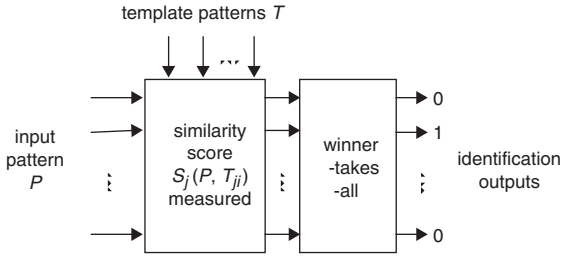

Fig. 13 *Pattern identification application*

function is obtained if the polarities of the *max/min-selector* signals are reversed.

(iv) Hybrid mode: Depending on application requirements, the *max/min-selector* signals in each circuit are different. This allows easy adaptation for special applications.

4.3 Pattern identification

A similarity measurement (SM) circuit is easily embedded within the WTA/LTA circuit for a pattern identification system. Figure 13 shows the conceptual diagram. The first block of Fig. 13 represents a SM circuit. Assuming there is an input pattern $\boldsymbol{P}$ with m elements $\langle p_1, p_2, \ldots, p_m \rangle$ and n template patterns $\langle T_{11}, T_{12}, \ldots, T_{1m} \rangle$, …, and $\langle T_{n1}, T_{n2}, \ldots, T_{nm} \rangle$. The score $S_i(p_j, T_{ij})$ is used to measure the similarity between input pattern $\boldsymbol{P}$ and i template pattern. An average of absolute differential value represents one of many $S_i(p_j, T_{ij})$ scores. The Hamming metric is represented as

$$S_i(p_j, T_{ij}) = \frac{1}{m} \sum_{j=1}^{m} |p_j - T_{ij}|, \quad i = 1 \ldots n \qquad (9)$$

For analogue pattern identification, the value of each element in an analogue pattern is an analogue level. Realisation of the SM circuit was shown in [20]. For binary pattern identification, the SM circuit is realised using the exclusive-NOR function [21]. Pattern identification, based on these SM circuits and WTA/LTA co-operation is thus realised.

5 Conclusions

This paper has presented a high-reliability CMOS WTA/LTA circuit with programmable capability. A WTA or LTA function is selected by an enable signal. Single-comparator architecture was proposed to reduce circuit sensitivity to process variation. Since the design of this architecture is not critical, circuit realisation using traditional CMOS technology is easy. The WTA/LTA circuit was shown to operate over a wide supply voltage range and a rail-to-rail input range; thus, the circuit is flexible and can be integrated with a similarity measurement circuit for pattern identification. Importantly, the circuit can be expanded to two-layer architecture to further reduce response time. Measured results on an experimental chip showed that 10 mV input difference was distinguished, and that 5 mV was obtainable at the cost of reduced operating speed.

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